Electronic Version
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Claims

[c1] 1. A method of fabricating a flash memory cell, comprising the steps of:
providing a substrate;
forming a patterned mask layer over the substrate;
etching the substrate using the patterned mask layer as an etching mask to form a trench in the substrate;
forming a first dielectric layer over the substrate;
forming a first gate and a second gate beside the respective sidewall of the trench, wherein the first gate and the second gate are at a distance from each other and expose a portion of the first dielectric layer at the bottom of the trench;
forming a first source/drain region in the substrate at the bottom of the trench;
forming a second dielectric layer over the substrate;
forming a passivation layer over the second dielectric layer;
removing a portion of the passivation layer, the second dielectric layer and the first dielectric layer to expose the substrate surface at the bottom of the trench;
forming a third gate that completely fills the trench;
removing the mask layer;

forming a third dielectric layer over the substrate;
forming a fourth gate and a fifth gate beside the respective sidewall of the first gate and the second gate; and
forming a second source/drain region in the substrate on one side of the fourth gate and the fifth gate.

[c2] 2. The method of claim 1, wherein material constituting the passivation layer comprises a semiconductor material or a conductive material.

[c3] 3. The method of claim 1, wherein a material constituting the passivation layer comprises undoped polysilicon.

[c4] 4. The method of claim 3, wherein the step of forming the passivation layer comprises performing a chemical vapor deposition process.

[c5] 5. The method of claim 3, wherein the passivation layer has a thickness of about 100Å.

[c6] 6. The method of claims 1, wherein a material constituting the first gate, the second gate, the third gate, the fourth gate and the fifth gate comprises undoped polysilicon.

[c7] 7. The method of claim 1, wherein the first gate and the second gate are floating gates, the third gate is a control gate, and the fourth gate and the fifth gate are select

gates.

[c8] 8. The method of claim 1, wherein each of the fourth gate and the fifth gate comprises a doped polysilicon layer and a metal silicide layer.

[c9] 9. The method of claim 1, wherein the first dielectric layer is a tunneling oxide layer and the second dielectric layer and the third dielectric layer are both inter-gate dielectric layer.

[c10] 10. The method of claim 1, wherein the step of forming the first gate and the second gate on the respective sidewall of the trench comprises:
depositing conductive material into the trench to form a conductive layer;
performing an etching back operation so that a top section of the conductive layer is at a level lower than a surface of the mask layer;
forming spacers on the sidewalls of the trench so that a portion of the conductive layer is covered; and
removing a portion of the conductive layer using the spacers and the mask layer as an etching mask to form the first gate and the second gate beside the respective sidewall of the trench.

[c11] 11. The method of claim 1, wherein the step of forming

the first gate and the second gate on the sidewalls of the trench comprises:

depositing a conductive material into the trench to form a conductive layer;

removing the conductive layer over the upper surface of the mask layer; and

patterning the conductive layer to form a first gate and a second gate beside the respective sidewall of the trench.

[c12] 12. The method of claim 1, further comprising a step of forming liner layer over the substrate before the step of forming the patterned mask layer over the substrate, and a step of removing the liner layer during the step of removing the mask layer.

[c13] 13. The method of claim 12, wherein a material constituting the liner layer comprises silicon oxide and a material constituting the mask layer comprises silicon nitride.

[c14] 14. The method of claim 1, further comprising a step of forming a fourth dielectric layer over the substrate before the step of forming the patterned mask layer over the substrate.

[c15] 15. A method of fabricating a flash memory cell, comprising the steps of:

providing a substrate, having a liner layer and a mask layer formed thereon, wherein an opening is formed in the liner layer and the mask layer and a trench is formed in the substrate below the opening;

forming a tunneling oxide layer on a surface of the trench;

depositing conductive material into the trench to form a conductive layer;

performing a etching back process so that a top section of the conductive layer is at a level higher than an upper surface of the liner layer but lower than an upper surface of the mask layer;

forming a pair of spacers on the respective sidewall of the trench so that a portion of the conductive layer is covered;

removing a portion of the conductive layer using the spacers and the mask layer as an etching mask to form a first floating gate and a second floating gate on the respective sidewall of the trench;

forming a first source/drain region in the substrate at a bottom of the trench;

forming a first inter-gate dielectric layer on the substrate and over a surface of the trench;

forming a passivation layer over the first inter-gate dielectric layer;

removing portions of the passivation layer, the first in-

ter-gate dielectric layer and the tunneling oxide layer until a portion of the substrate at the bottom of the trench is exposed;

forming a control gate that completely fills the trench, wherein a top section of the control gate is at a level higher than a top section of both the first floating gate and the second floating gate;

removing the liner layer and the mask layer;

forming a second inter-gate dielectric layer over the substrate;

forming a first select gate and a second select gate beside the respective sidewall of the spacers, the first floating gate and the second floating gate; and

forming a second source/drain region in the substrate on one side of the first select gate and the second select gate.

[c16] 16. The method of claim 15, wherein a material constituting the passivation layer comprises a semiconductor material or a conductive material.

[c17] 17. The method of claim 15, wherein a material constituting the passivation layer comprises undoped polysilicon.

[c18] 18. The method of claim 17, wherein the step of forming the passivation layer comprises performing a chemical

vapor deposition process.

[c19] 19. The method of claim 17, wherein a material constituting the conductive layer and the control gate comprises doped polysilicon.

[c20] 20. The method of claim 15, wherein the first inter-gate dielectric layer is a composite stack structure comprising a silicon oxide layer, a silicon nitride layer and another silicon oxide layer.

[c21] 21. The method of claim 15, wherein a material constituting the second inter-gate dielectric layer comprises a silicon oxide.

[c22] 22. The method of claim 15, wherein each of the first select gate and the second select gate comprise a doped polysilicon layer and a metal silicide layer.

[c23] 23. The method of claim 15, wherein a material constituting the liner layer comprises silicon oxide and a material constituting the mask layer comprises silicon nitride.